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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,158	08/28/2001	William R. Wheeler	10559-596001 / P12880	4619

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/941,158	Applicant(s) WHEELER ET AL.
	Examiner Stacy A Whitmore	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *26-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-25, in Paper No. 7, is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 13 and 25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

3. Claims 13 and 25 include the limitation "code ordering" which is described in the specification, page 6, lines 16-17, to mean that logical constructs are sorted based on producer/consumer. The examiner interprets this definition as being non-enabling because the phrase "producer/consumer" does not fully describe what "code ordering" is.

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
In claims 13 and 25, the term "code ordering" is unclear because as disclosed in the specification on page 6, lines 16-17, the phrase "producer/consumer" does not fully describe what "code ordering" is.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-10, 14, and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandell (US Patent 6,477,689) in view of Reynolds (US Patent 6,480,985).

6. As for claims 1, and 5-6, Mandell disclosed the invention substantially as claimed, including a method for designing a logic circuit comprising:

maintaining a data structure representative of a model [col. 1, lines 21-23; col. Col. 7, lines 12-28];

the model including combinational blocks [col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements] and

generating an architectural model (C code) and an implementation model (HDL) from the data structure [col. 7, lines 29-32, especially the generation of HDL and C-code].

Mandell did not specifically disclosed C++ code or the model including state elements and graphical library elements of the logic circuit.

Reynolds disclosed C++ code and a model including state elements and graphical library elements (graphical representations which are stored in a file or library format) of the logic circuit [abstract; col. 7, lines 14-17; and col. 8, lines 44-49; and col. 12, lines 35-42].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because Reynolds use of C++ code would have improved Mandell's system by providing a more object oriented model which would be useful for providing graphical representations of the circuit for ease of use by a user. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Reynolds state elements and graphical library elements because having Reynold's state elements would have provided a way of state transitions for circuit simulation or verification and the graphical elements would have provided for an easier design system for a user by providing visual and interactive design through a user interface [see Reynolds col.'s 7 and 8].

7. As for claim 2, Mandell further disclosed wherein the data structure comprises a description of a net list [col. 7].

8. As for claims 7 and 8, as applied to claims 1 and 6, Mandell and Reynolds disclosed the invention substantially as claimed, including the method for designing a logic circuit as cited in the rejection of claims 1 and 6. Reynolds further disclosed

wherein the HDL is Verilog and wherein the HDL is Very high speed integrated circuit Hardware Design Language (VHDL) [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because using Reynold's VHDL or Verilog would have allowed a circuit designer to use high level code which would be advantageous for changing circuit designs [see Reynolds; col. 1, lines 13-40]

9. As for claim 9, Mandell disclosed the invention substantially as claimed, including a method comprising:

specifying a model containing combinatorial blocks [col. 1, lines 21-23; col. Col. 7, lines 12-28; col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements];

maintaining a descriptive net list of the model [col. 7]; and

generating a C model and a HDL model from the descriptive net list [col. 7, lines 29-32, especially the generation of HDL and C-code].

Mandell did not specifically disclose specifying state elements and graphical library elements and generating C++ and Verilog.

However, Reynolds disclosed specifying state elements and graphical library elements (graphical representations which are stored in a file or library format) and generating C++ and Verilog of the logic circuit [abstract; col. 7, lines 14-17; and col. 8, lines 44-49; and col. 12, lines 35-42].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because Reynolds use of C++ code would have improved Mandell's system by providing a more object oriented model which would be useful for providing graphical representations of the circuit for

ease of use by a user. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Reynolds state elements and graphical library elements because having Reynold's state elements would have provided a way of state transitions for circuit simulation or verification and the graphical elements would have provided for an easier design system for a user by providing visual and interactive design through a user interface [see Reynolds col.'s 3, 7 and 8].

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because using Reynold's VHDL or Verilog would have allowed a circuit designer to use high level code which would be advantageous for changing circuit designs [see Reynolds; col. 1, lines 13-40]

10. As for claim 10, Reynolds further disclosed displaying the model on a graphical user interface (GUI) [col. 1, lines 46-49; col. 2, lines 45-57].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because providing a display of the model on a graphical user interface would have improved Mandell's system by more effectively communicating the functionality of the circuit by the designer which would improve design efficiency [see Reynolds; col. 1, liens 48-50].

11. As for claim 14, Mandell disclosed the invention substantially as claimed, including a computer program product residing on a computer readable medium [abstract] a having instructions stored thereon which, when executed by the processor, cause the processor to:

specify a model containing combinatorial blocks [col. 1, lines 21-23; col. Col. 7, lines 12-28; col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements];

maintain a descriptive net list of the model [col. 7]; and

generate a C model and a HDL model from the descriptive net list [col. 7, lines 29-32, especially the generation of HDL and C-code].

Mandell did not specifically disclose specifying state elements and graphical library elements and generating C++ and Verilog, and [claims 15-17 wherein the computer readable medium is a RAM, RAM or hard disk drive].

Reynolds disclosed specifying state elements and graphical library elements (graphical representations which are stored in a file or library format) and generating C++ and Verilog of the logic circuit [abstract; col. 7, lines 14-17; and col. 8, lines 44-49; and col. 12, lines 35-42]; and [claims 15-17 wherein the computer readable medium is a RAM, RAM or hard disk drive; col. 2, lines 58-58; col. 3, lines 3-9]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because Reynolds use of C++ code would have improved Mandell's system by providing a more object oriented model which would be useful for providing graphical representations of the circuit for ease of use by a user. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Reynolds state elements and graphical library elements because having Reynold's state elements would have provided a way of state transitions for circuit simulation or verification and the graphical elements would have provided for an easier design system for a user by providing visual and interactive design through a user interface [see Reynolds col.'s 3, 7 and 8].

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because using Reynold's VHDL or Verilog would have allowed a circuit designer to use high level code which would be advantageous for changing circuit designs [see Reynolds; col. 1, lines 13-40].

Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because having devices such as Reynold's RAM, ROM and hard disk drive are well known in the art for storing computer program products for the purpose of data storage as well as program execution and would have provided a necessary function of storing program data for executing Mandell's design tool.

12. As for claims 18-21, Mandell disclosed the invention substantially as claimed, including a processor and memory [abstract] [claims 19-21; wherein the processor and memory are incorporated into a personal computer; wherein the processor and memory are incorporated into a network server residing in the Internet; wherein the processor and memory are incorporated into a single board computer col. 2-3] configured to:

specify a model containing combinatorial blocks, maintain a descriptive net list of the model [col. 1, lines 21-23; col. Col. 7, lines 12-28; col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements; and col. 7]; and

generate a C model and a HDL model from the descriptive net list [col. 7, lines 29-32, especially the generation of HDL and C-code].

Mandell did not specifically disclose specifying state elements and graphical library elements and generating C++ and Verilog.

Reynolds disclosed specifying state elements and graphical library elements (graphical representations which are stored in a file or library format) and generating C++ and Verilog of the logic circuit [abstract; col. 7, lines 14-17; and col. 8, lines 44-49; and col. 12, lines 35-42].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because Reynolds use of C++ code would have improved Mandell's system by providing a more object oriented

model which would be useful for providing graphical representations of the circuit for ease of use by a user. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Reynolds state elements and graphical library elements because having Reynold's state elements would have provided a way of state transitions for circuit simulation or verification and the graphical elements would have provided for an easier design system for a user by providing visual and interactive design through a user interface [see Reynolds col.'s 3, 7 and 8].

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because using Reynold's VHDL or Verilog would have allowed a circuit designer to use high level code which would be advantageous for changing circuit designs [see Reynolds; col. 1, lines 13-40].

13. As for claim 22, Reynolds disclosed the invention substantially as claimed, including a system comprising:

generating a model , the model containing combinatorial blocks [col. 1, lines 21-23; col. Col. 7, lines 12-28; col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements; and col. 7]

a graphic user interface (GUI) for receiving parameters from a user to generate a model and displaying the model, the model containing combinatorial blocks, state elements and graphical library elements;

a maintenance process to manage a data structure representing a descriptive net list of the model [col. 1, lines 21-23; col. Col. 7, lines 12-28; col. 3, lines 51-54 – especially parts which includes the representations of various combinations of circuit elements; and col. 7]; and

a code generation process to generate a C model and a HDL model from the data structure [col. 7, lines 29-32, especially the generation of HDL and C-code].

Mandell did not specifically disclose specifying state elements and graphical library elements and generating C++ and Verilog and a graphical user interface for receiving parameters from a user to generate a model.

Reynolds disclosed specifying state elements and graphical library elements (graphical representations which are stored in a file or library format) and generating C++ and Verilog of the logic circuit [abstract; col. 7, lines 14-17; and col. 8, lines 44-49; and col. 12, lines 35-42] and a graphical user interface for receiving parameters from a user to generate a model [col. 1, lines 46-49; col. 2, lines 45-57].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because Reynolds use of C++ code would have improved Mandell's system by providing a more object oriented model which would be useful for providing graphical representations of the circuit for ease of use by a user. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Reynolds state elements and graphical library elements because having Reynold's state elements would have provided a way of state transitions for circuit simulation or verification and the graphical elements would have provided for an easier design system for a user by providing visual and interactive design through a user interface [see Reynolds col.'s 3, 7 and 8].

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because using Reynold's VHDL or Verilog would have allowed a circuit designer to use high level code which would be advantageous for changing circuit designs [see Reynolds; col. 1, lines 13-40].

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell and Reynolds because providing a graphical user interface for receiving parameters from a user to generate a

model would have improved Mandell's system by more effectively communicating the functionality of the circuit by the designer which would improve design efficiency [see Reynolds; col. 1, liens 48-50].

14. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandell (US Patent 6,477,689) in view of Reynolds (US Patent 6,480,985), as applied to claims 1-2 above, and further in view of Liao et al. (US Patent 6,152,612).

15. As for claims 3-4, Mandell in view of Reynolds disclosed the invention substantially as claimed, including the method of for designing a logic circuit [see as cited in the rejections of claims 1-2] and further disclosed wherein the data structure comprises:

> elements representing logical functions [see Mandell, col. 3, lines 50-55, especially logical connections of nets];
> elements representing connection points to gates [see Mandell, col. 3, lines 50-55, especially logical connections of "points" which are the gates; and also col. 7, lines 13-27, especially input and output ports, which are the gates]; and a state machine [see Reynolds col. 7, line 14-17].

Mandell in view of Reynolds did not specifically disclose elements representing all bits of a simulation state; and elements representing an arbitrary collection of bits within the simulation state.

Liao disclosed elements representing all bits of a simulation state; and elements representing an arbitrary collection of bits within the simulation state and that the elements are all C++ classes [col. 9, especially class FSM, constant and variable (arbitrary) bits of simulation states; and col. 6].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell in view of Reynolds, and Liao because Mandell in view of Reynolds, and Liao disclosed the use of C++ and state machines [see Reynolds col.'s 7 and 8; see Liao, col. 9.] Furthermore, the use of C++ classes as well as representing the bits within a simulation state would have improved Mandell in view of Reynolds system by allowing circuit designers to easily map their models to widely available tools for hardware implementation [see Liao, col. 6, lines 40-67]

16. Claims 11-12, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandell (US Patent 6,477,689) in view of Reynolds (US Patent 6,480,985), as applied to claims 9 and 22 above, and further in view of Anderson (US Patent 6,519,755).

17. As for claims 11-12 and 23-25, Mandell in view of Reynolds disclosed the invention substantially as claimed, including the method of specifying a model and generating a C++ model and Verilog model including combinatorial blocks, state elements, and graphical library elements as cited in the rejection of claim 9 above, and further disclosed wherein the net list comprises nets [see Mandell col. 3, line 54].

Mandell in view of Reynolds did not disclose that the netlist comprises gates and nodes, and parsing and analyzing the elements

Anderson disclosed that the netlist comprises gates and nodes [col. 6] and parsing and analyzing the elements [col. 5, lines 16; fig. 28; and col. 10, line 55 – col. 11, line 5].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Mandell in view of Reynolds, and Anderson because gates and nodes are well known elements in circuit designs and having well known circuit elements in the netlist would have allowed for the representation of elements that are a normal part of circuit models.

Furthermore, It would have been obvious to one of ordinary skill in the art to combine the teachings of Mandell in view of Reynolds, and Anderson because parsing and analyzing the elements would have improved Mandell in view of Reynolds system by providing a method of representing elements in a word oriented database which would allow for objects to be easily represented as values such as integers which are easier to use than bit oriented constructs [see Anderson, col. 10, line 55 – col. 11, line 5]

18. Claims 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandell (US Patent 6,477,689) in view of Reynolds (US Patent 6,480,985), as applied to claims 9 and 22 above, and further in view of Seawright (US 2002/0023256).

19. As for claims 13 and 25, Mandell in view of Reynolds disclosed the invention substantially as claimed, including the method of specifying a model and generating a C++ model and Verilog model including combinatorial blocks, state elements, and graphical library elements as cited in the rejection of claim 9 above, and further disclosed wherein the net list comprises nets [see Mandell col. 3, line 54].

Mandell in view of Reynolds did not specifically disclose partitioning a topology of the net list into a plurality of partitions; and code ordering each of the partitions.

Seawright disclosed partitioning a topology of the net list into a plurality of partitions; and code ordering each of the partitions [fig.'s 4-5; pg. 3-4, paragraphs 45-51].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Mandell in view of Reynolds, and Seawright because Mandell in view of Reynolds, and Seawright all disclose the circuit design using hardware descriptions which would benefit by Seawright partitioning and code ordering of the netlist topology because Seawrights partitioning process optimizes the hardware description which would improve design and Seawright code ordering

(recoding) the partitions would be necessary for recoding the optimized hardware descriptions.

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,053,947	Parson	C++ classes
6,135,647	Balakrishnan	GUI, C++ library files, C++ classes, Verilog and other circuit descriptions
US 2003/0016246	Singh	library graphical class
US 2003/0016206	Taitel	GUI, TCP/IP, C code
6,233,540	Schaumont	behavioral and implementable descriptions, objects, finite state machines, C++, HDL, clock cycle, simulation
6,487,698	Andreev	Verilog, C++

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW
March 7, 2003